Jie Liu

jl3952@cornell.edu • +1 (607) 216-7193
Website • Scholar • Profile • Sibylau

RESEARCH INTERESTS

• Compilers • Domain-Specific Languages • Sparse Data Processing • Heterogeneous Computing
My research objective is to facilitate automatic optimizations for processing sparse data on heterogeneous platforms by establishing a unified abstraction that represents custom sparse formats.

EDUCATION

Cornell University, Ithaca, NY, USA

- Ph.D. Candidate in Computer Systems Lab, ECE — Aug 2019 – Jan 2025 (Expected)
  - Advisor: Prof. Zhiru Zhang
  - Courses: Computer Architecture (A), Complex Digital ASIC Design (A), Advanced Compilers (A), Computer Systems Language (Teaching Assistant)

Tsinghua University, Beijing, China

- B.Eng in Microelectronic Science and Engineering — Sep 2015 – Jul 2019
  - Overall GPA: 3.62/4.0; Rank: 5/24
- Minor in Financial Engineering — Sep 2017 – Jul 2019

PROFESSIONAL EXPERIENCE

Microsoft Research, Redmond, WA, USA

- Research Intern — May 2024 – Aug 2024

Pacific Northwest National Laboratory (PNNL), Richland, WA, USA

- PhD Intern — May 2023 – Aug 2023

AMD Xilinx, Inc., San Jose, CA, USA

- Compiler Intern at Xilinx Research Labs — May 2021 – Aug 2021

University of California, Los Angeles (UCLA), Los Angeles, CA, USA

- Undergraduate Research Intern at the VAST Laboratory — Jun 2018 – Sep 2018
  - Advisor: Prof. Jason Cong

RESEARCH PROJECTS

Compiler Optimizations for GPU Database
Research Intern, with Kaushik Rajan, Microsoft Research — May 2024 – Aug 2024

- Extend the MLIR-based compiler framework for GPU database.
- Characterize the performance bottlenecks and identify optimization opportunities.

A Unified Abstraction for General Sparse Format Customization on Heterogeneous Platforms
Ph.D. student, with Prof. Zhiru Zhang, Cornell University — Dec 2021 – Dec 2023

- Proposed a unified tensor format abstraction that expresses both classic and custom hardware-friendly sparse formats.
- Implemented a compiler flow based on the MLIR framework that automatically converts tensor formats and generates sparse processing kernels.

A Programming Abstraction for Reconfigurable Dataflow Architectures
Ph.D. Intern, with Dr. Gokcen Kestor, PNNL — May 2023 – Oct 2023

- Proposed a programming attraction for reconfigurable dataflow architectures.
- Implemented a dataflow dialect based on the MLIR framework that lowers from the front-end linear algebra programs to the SambaNova programming interface.

Automatic Loop Scheduling for Spatial Architectures
Compiler Intern, with Dr. Stephen Neuendorffer, AMD Xilinx, Inc. — May 2021 – Aug 2021

- Proposed an ILP model to solve for optimal mapping solutions from algorithmic loops to spatial architectures under given resource constraints.
- Implemented an automatic loop scheduling flow configured by results of the ILP solver as part of the MLIR AIEngine toolchain.

Backend Optimization for HeteroCL
Ph.D. student, with Prof. Zhiru Zhang, Cornell University — Sep 2020 – May 2021

- Implemented a loop unrolling pass at the LLVM IR level for HeteroCL.
- Implemented a Mentor Graphics Catapult High-Level Synthesis (HLS) backend for HeteroCL.

A Row-Wise Product Based Sparse-Sparse Matrix Multiplication Accelerator
Ph.D. student, with Prof. Zhiru Zhang, Cornell University — Nov 2019 – Sep 2020

- Involved in the design of a hardware-friendly sparse format and a row-wise product based specialized accelerator architecture for sparse-sparse matrix multiplication (SpGEMM).
- Implemented the accelerator using PyMTL and Mentor Graphics Catapult HLS tool.

Systolic Array Design Implementation for Matrix Decomposition Algorithms
Undergraduate Research Intern, with Prof. Jason Cong, UCLA — Jul 2018 – Oct 2018

- Designed 1D and 2D highly-optimized systolic array architectures based on polyhedral analysis theory using Xilinx Vivado HLS tools.
- Achieved up to 50.13x and 4.58x better throughput compared with the Xilinx HLS linear algebra library and the LAPACK library on single-thread CPUs.

IMU-based System for Real-Time Pelvis Plane Measurement
Undergraduate Research Assistant, with Prof. Hong Chen, Tsinghua University — Oct 2017 – Apr 2018

- Built a pelvis position measurement system with IMU sensor modules, and optimized the position estimation algorithm for better accuracy and stability.

PROFESSIONAL SERVICES

Journal Reviewer

- ACM Transactions on Architecture and Code Optimization (TACO) — 2023
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) — 2023
- ACM Transactions on Reconfigurable Technology and Systems (TRETS) — 2023, 2024
- IEEE Journal of Biomedical and Health Informatics (JBHI) — 2024

TEACHING EXPERIENCE

Teaching Assistant

- ECE 2400: Computer Systems Language — spring 2024

SKILLS

Programming Languages: C/C++, Python, Matlab, Verilog / PyMTL, LaTeX, HSpice, SQL
Frameworks: MLIR / LLVM
CAD Tools: Mentor Catapult HLS, Cadence Stratus HLS, Xilinx Vitis HLS

HONORS & AWARDS

Jacobs Scholar Fellowship, Cornell University — 2019
Excellent SRT (Student Research Training) Project Award, Tsinghua University — 2019
Summer Overseas Research Training Scholarship, Tsinghua University — 2018

PUBLICATIONS

CONFERENCES

[1] J. Liu, Z. Zhao, Z. Ding, B. Brock, H. Rong, and Z. Zhang, **UniSparse: An Intermediate Language for General Sparse Format Customization**, *Object-Oriented Programming, Systems, Languages, and Applications 2024 (in PACMPL) (OOPSLA 2024)*

[2] N. Srivastava, H. Jin, J. Liu, D. Albonesi and Z. Zhang, **MatRaptor: A Sparse-Sparse Matrix Multiplication Accelerator Based on Row-Wise Product**, *2020 53rd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, Athens, Greece, 2020, pp. 766-780, DOI: 10.1109/MICRO50266.2020.00068.

JOURNALS

[1] J. Liu, Z. Zhao, Z. Ding, B. Brock, H. Rong and Z. Zhang, **An Intermediate Language for General Sparse Format Customization**, in *IEEE Computer Architecture Letters*, vol. 22, no. 2, pp. 153-156, July-Dec. 2023, DOI: 10.1109/LCA.2023.3262610.

[2] H. Chen, Z. Cao, S. Su, J. Liu and Z. Wang, **Measurement System for Attitude of Anterior Pelvic Plane and Implantation of Prothesis in THR Surgery**, in *IEEE Transactions on Instrumentation and Measurement*, vol. 67, no. 8, pp. 1913-1921, Aug. 2018, DOI: 10.1109/TIM.2018.2809818.

[3] H. Chen, Z. Yang, J. Zhang, J. Liu, H. Tang, Y. Zhou, B. Zhu, Z. Wang, **An IMU-Based Real-Time Measuring System for Acetabular Prosthesis Implant Angles in THR Surgeries**, in *IEEE Sensors Journal*, vol. 21, no. 17, pp. 19407-19415, 1 Sept.1, 2021, DOI: 10.1109/JSEN.2021.3091583.

POSTERS

[1] Jie Liu, Jason Cong, **Dataflow Systolic Array Implementations of Matrix Decomposition using High Level Synthesis**, *27th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2019)*, February 24-26, 2019, Monterey Bay Seaside, California, USA.

[2] Jie Liu, Hong Chen, Zhihua Wang, **IMU-based Real-Time Acetabular Prosthesis Implant Angles Measurement in Total Hip Replacement Surgeries**, *IEEE Biomedical Circuits and Systems Conference (BioCAS 2018)*, October 17-19, 2018, Cleveland, Ohio, USA.

WORKSHOPS

[1] Jie Liu, Zhongyuan Zhao, Zijian Ding, Benjamin Brock, Hongbo Rong, and Zhiru Zhang, **UniSparse: An Intermediate Language for General Sparse Format Customization**

- *The Workshop on Distributions, Relational Algebra, Graphs, Semi-Rings, Tensors, and All That (DRAGSTERS) of the 44th ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI'23)* Jun 2023
- *The Semiconductor Research Corporation (SRC) TECHCON* Sep 2023